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(54) **LIGHT-EMITTING DIODE DISPLAY PANEL AND DRIVING METHOD THEREOF**

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| ***G09G 3/3283*** | (2006.01) |

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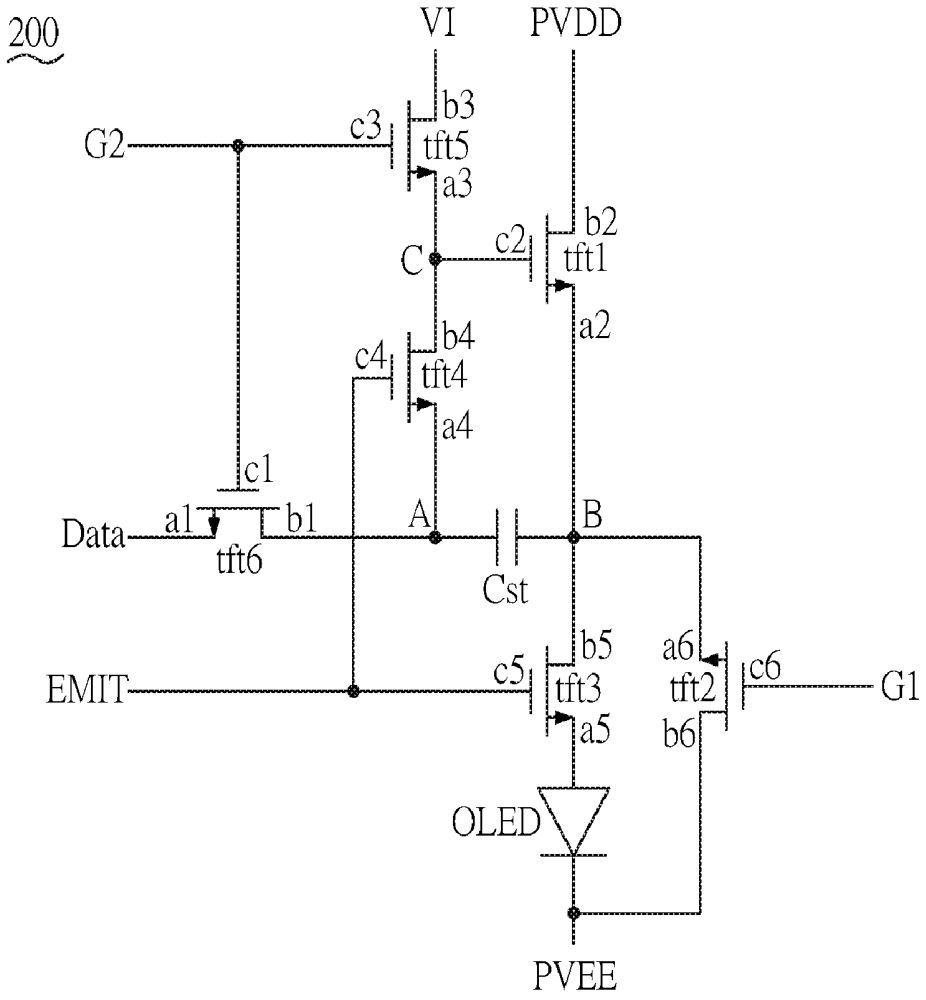
(57) **ABSTRACT**

The present disclosure provides a light-emitting diode display panel and the driving method thereof. Data transistor includes control terminal connected to first control signal source, first terminal connected to data line, and second terminal. Driving transistor includes control terminal, first terminal, and second terminal connected to high voltage source. Storage capacitor is connected to data and driving transistors. Compensating transistor includes control terminal connected to first control signal source, first terminal connected to control terminal of driving transistor, and second terminal connected to second control signal source. First control transistor includes control terminal connected to third control signal source, first terminal connected to second terminal of the data transistor, and second terminal connected to control terminal of driving transistor. Second control transistor includes control terminal connected to third control signal source, first terminal connected to organic light-emitting diode element, and second terminal connected to first terminal of driving transistor.



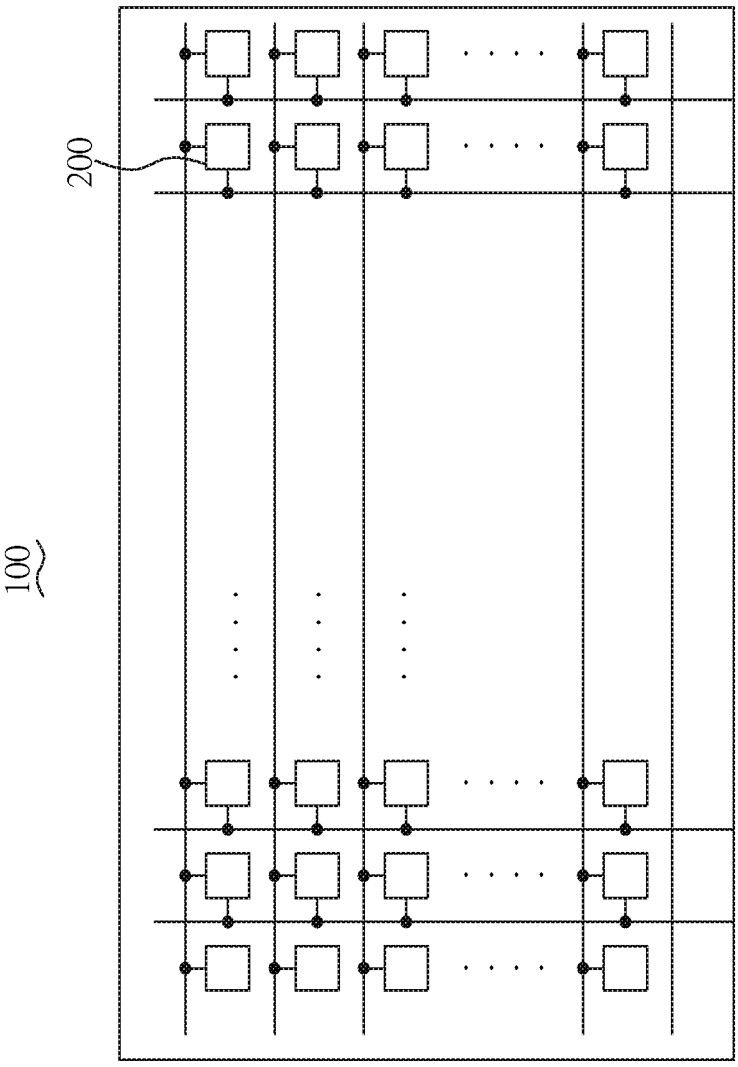



FIG. 1

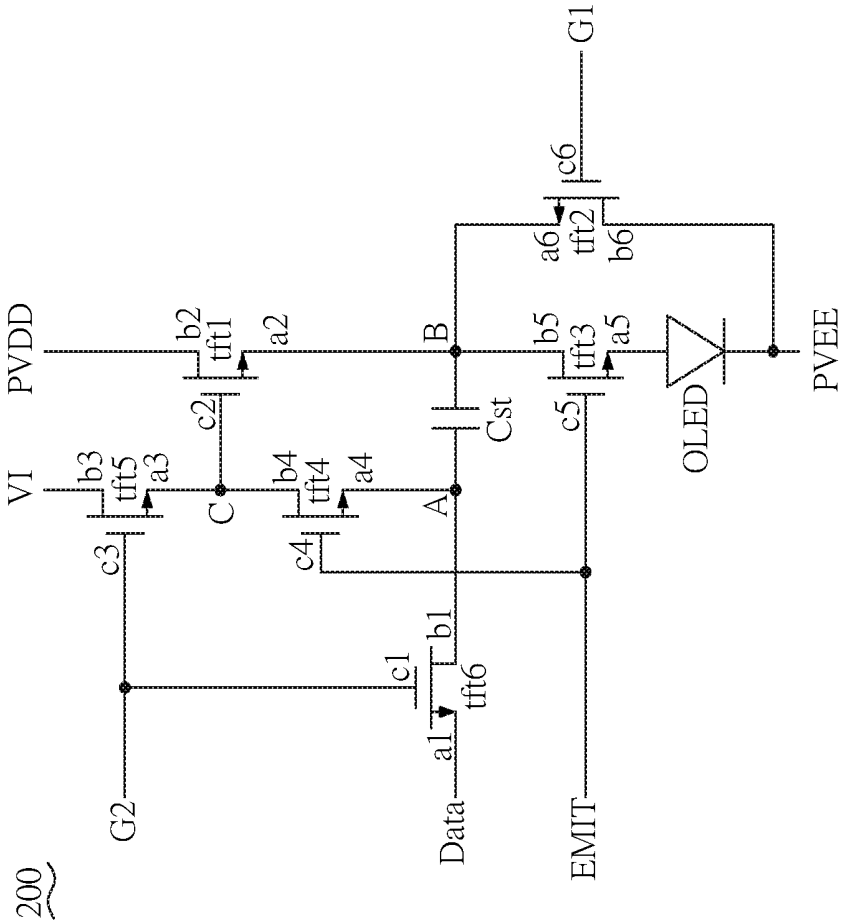

200
G2
Data
EMIT
G1
VI
PVDD
PVEE
OLED
Cst
A
B
C
tft1
tft2
tft3
tft4
tft5
tft6
a1
a2
a3
a4
a5
a6
b1
b2
b3
b4
b5
b6
c1
c2
c3
c4
c5
c6

FIG. 2

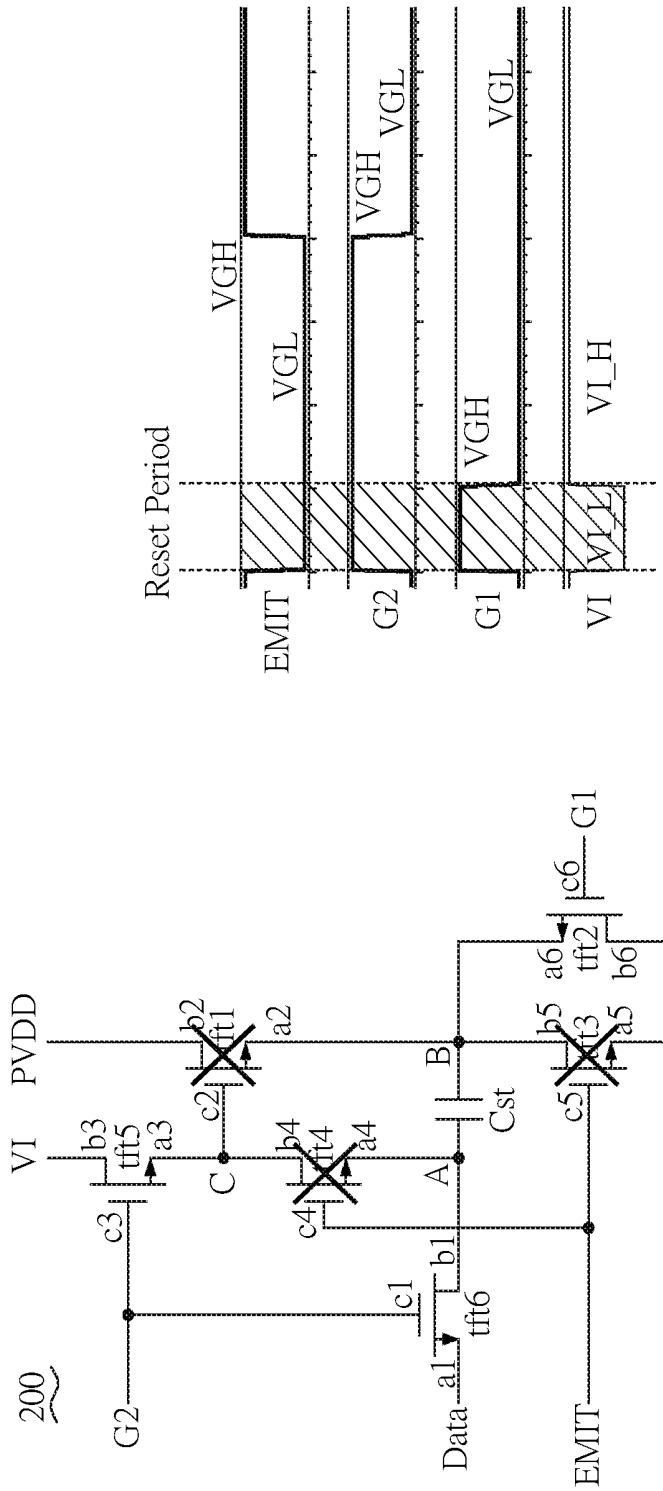

200
G2
Data
EMIT
PVDD
VI
PVEE
OLED
Cst
A
B
C
tft1
tft2
tft3
tft4
tft5
tft6
a1
a2
a3
a4
a5
a6
b1
b2
b3
b4
b5
b6
c1
c2
c3
c4
c5
c6
G1
Reset Period
VGH
VGL
VI_H
VI_L
EMIT
G2
G1
VI

FIG. 3

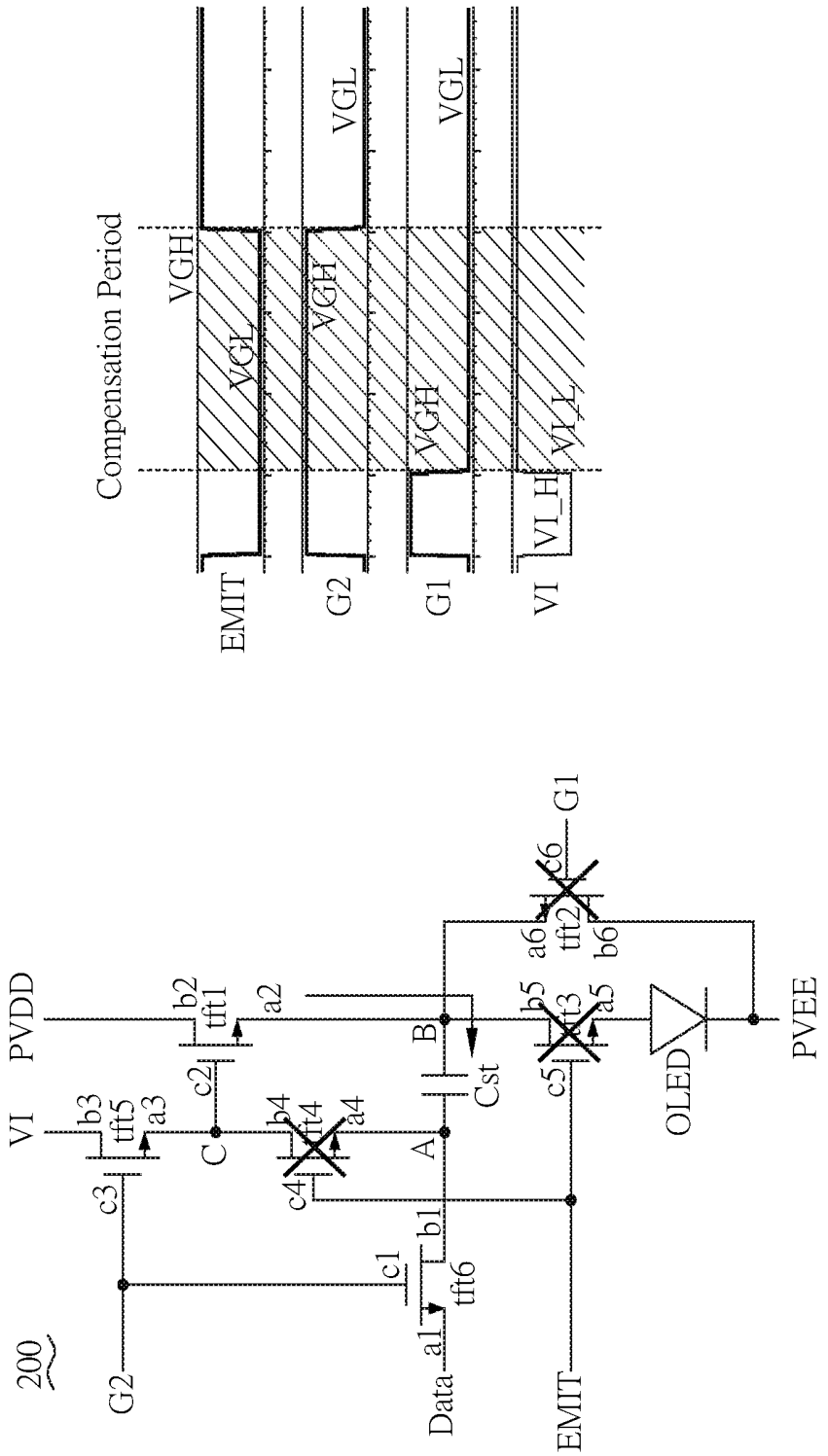
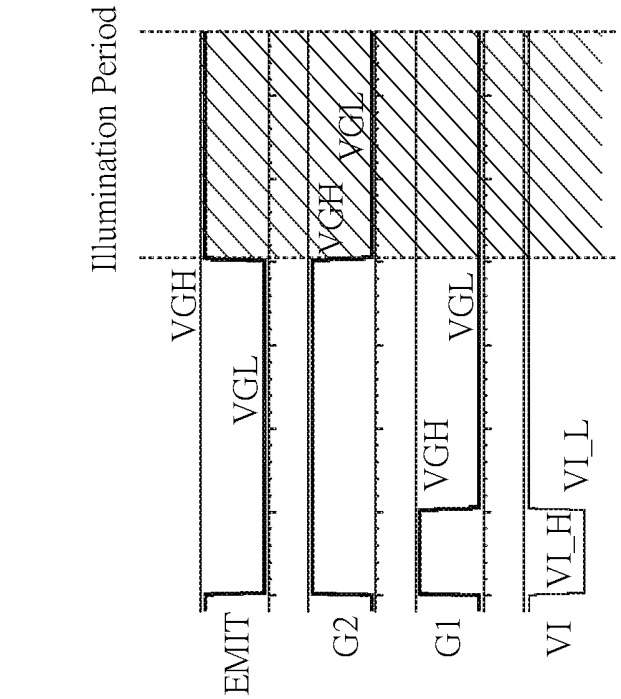

Compensation Period
VGH
VGL
VGH
VGL
VGH
VGL
VI_H
VI_L
EMIT
G2
G1
VI
200
G2
EMIT
Data
a1
tft6
b1
c1
c3
c4
tft4
a4
b4
C
c2
tft5
a3
b3
VI
A
B
Cst
c5
tft3
a5
b5
OLED
PVEE
PVDD
tft1
a2
b2
a6
tft2
b6
c6
G1

FIG. 4


Illumination Period
VGH
VGL
VGH
VGL
VGH
VGL
VI_H
VI_L
EMIT
G2
G1
VI

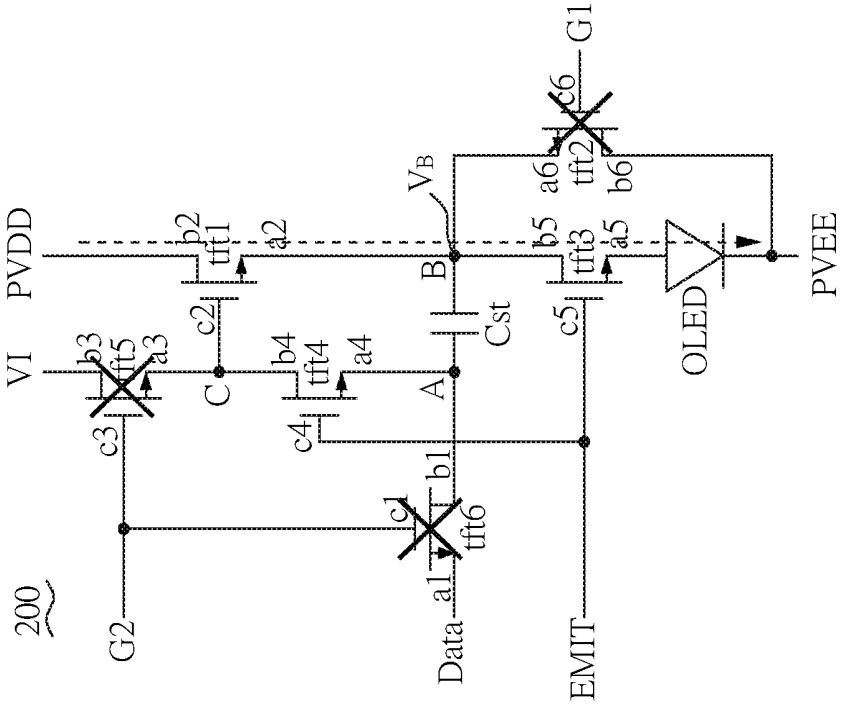

200
G2
Data
EMIT
VI
PVDD
PVEE
G1
OLED
Cst
A
B
C
$V_B$
tft1
tft2
tft3
tft4
tft5
tft6
a1
a2
a3
a4
a5
a6
b1
b2
b3
b4
b5
b6
c1
c2
c3
c4
c5
c6

FIG. 5

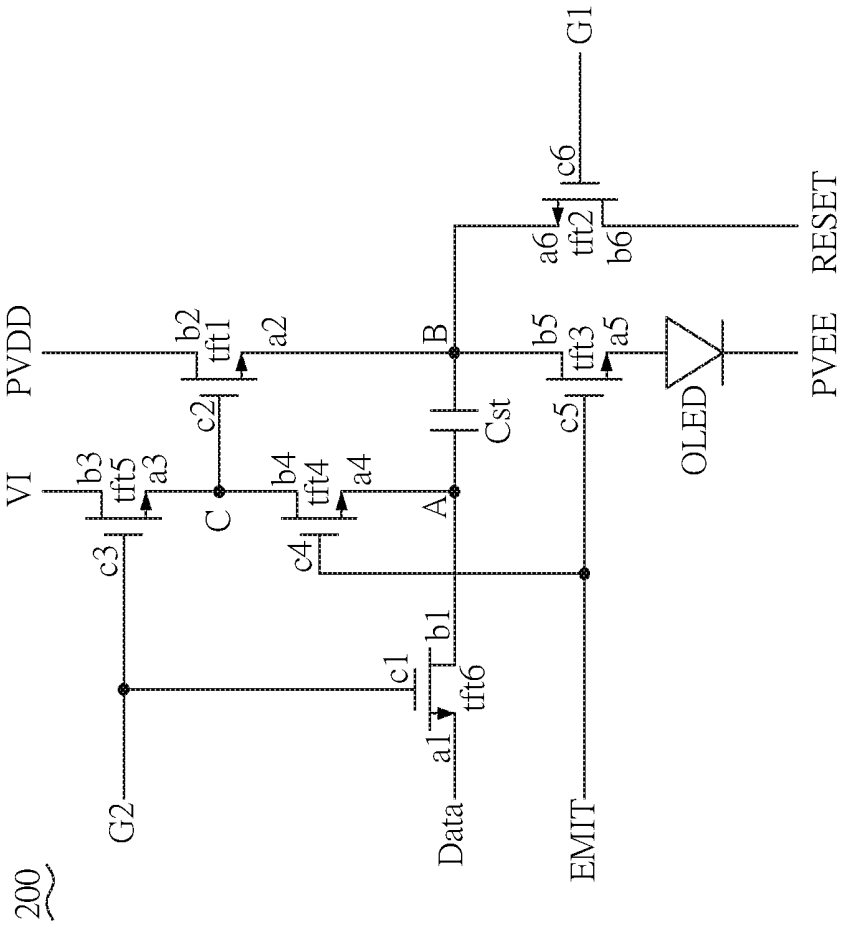

200
G2
Data
EMIT
PVDD
VI
C
A
B
Cst
OLED
PVEE
RESET
G1
c1
c2
c3
c4
c5
c6
a1
a2
a3
a4
a5
a6
b1
b2
b3
b4
b5
b6
tft6
tft1
tft5
tft4
tft3
tft2

FIG. 6

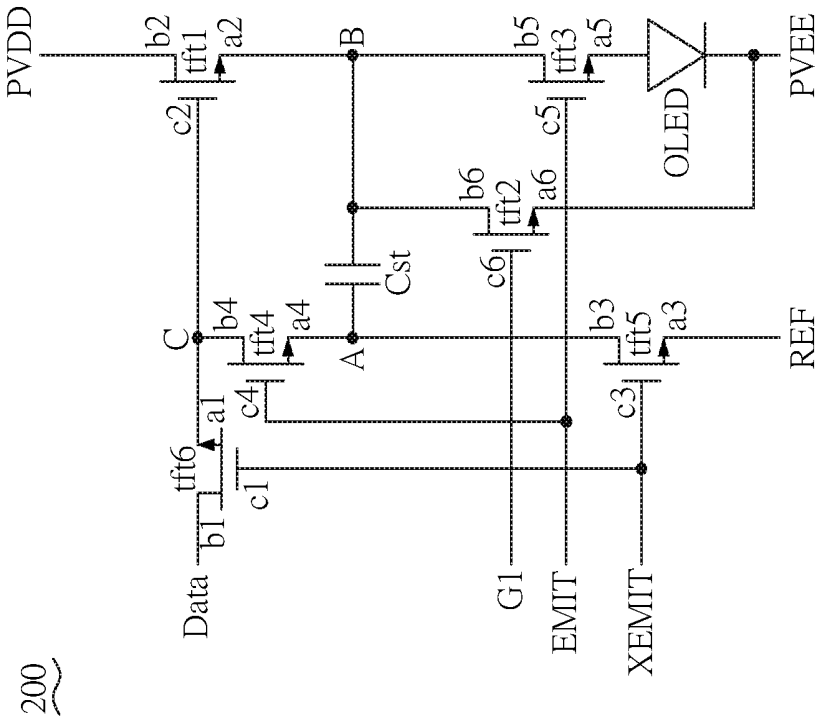

200
PVDD
b2
tft1
a2
B
b5
tft3
a5
PVEE
c2
c5
OLED
b6
tft2
a6
c6
Cst
C
b4
tft4
a4
A
b3
tft5
a3
REF
c4
c3
a1
tft6
c1
b1
Data
G1
EMIT
XEMIT

FIG. 7

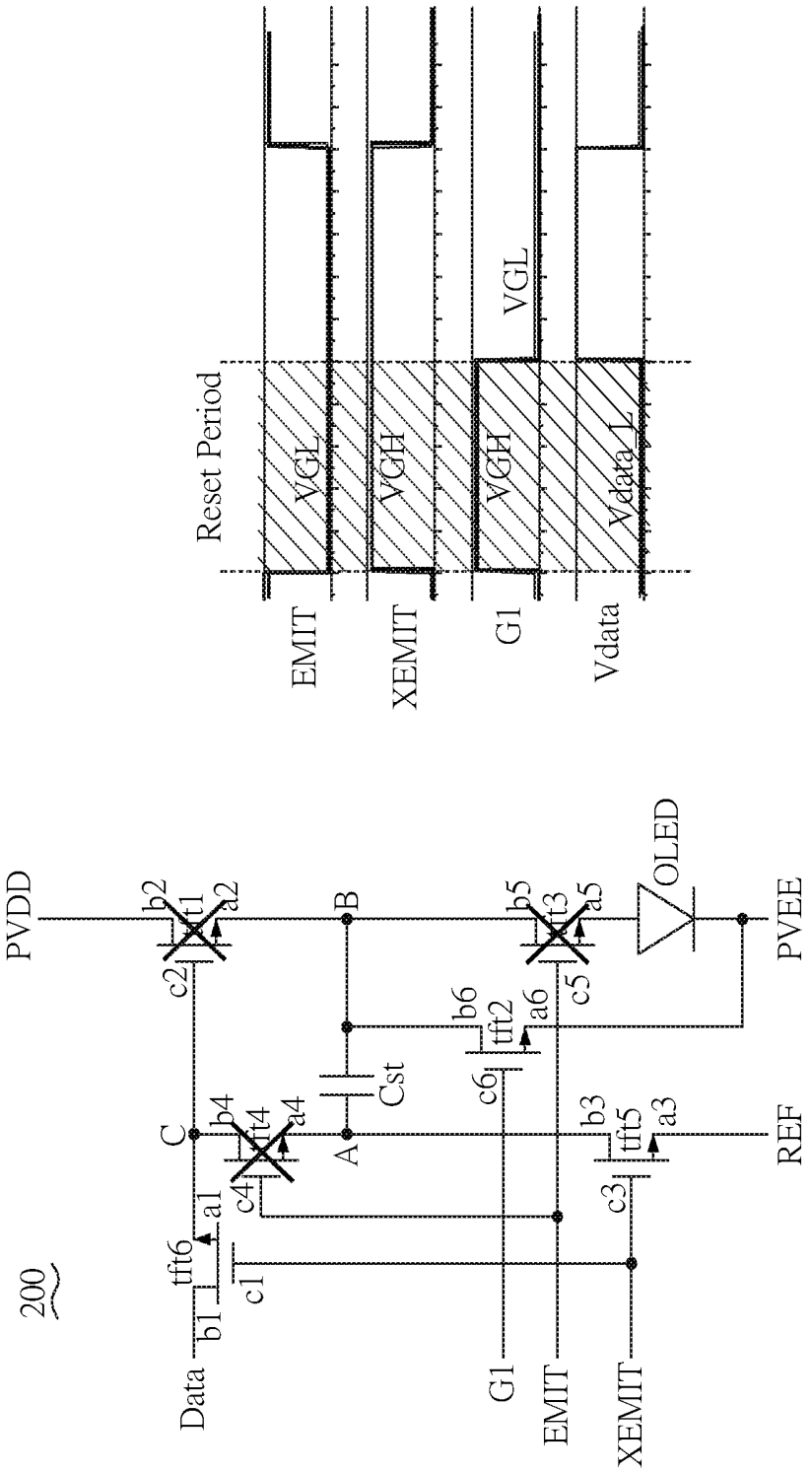

Reset Period
VGL
VGH
VGH
Vdata
VGL
EMIT
XEMIT
G1
Vdata
200
PVDD
PVEE
OLED
B
C
A
Cst
REF
Data
G1
EMIT
XEMIT
tft1
tft2
tft3
tft4
tft5
tft6
a1
a2
a3
a4
a5
a6
b1
b2
b3
b4
b5
b6
c1
c2
c3
c4
c5
c6

FIG. 8

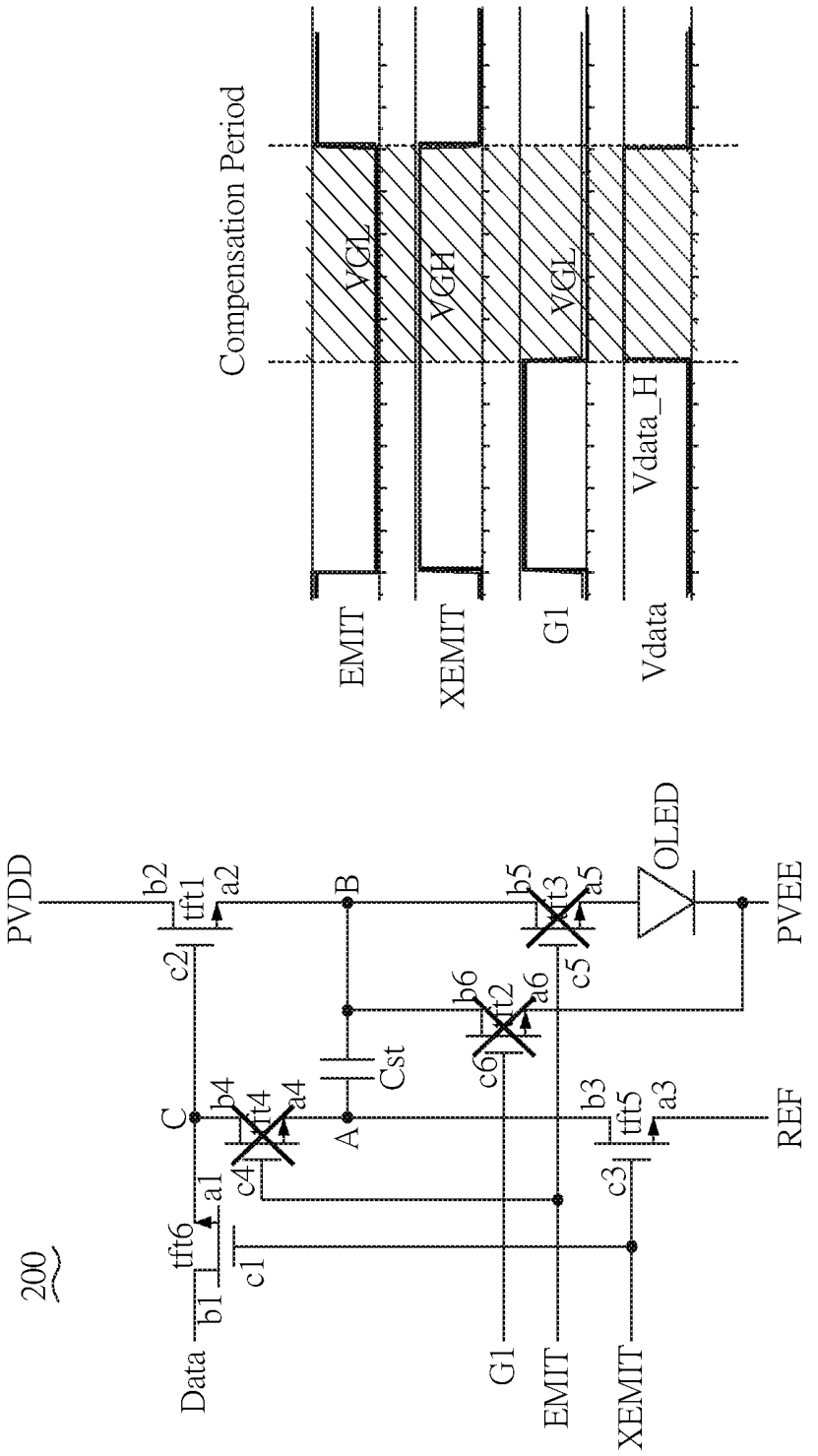

Compensation Period
VGL
VGH
VGL
Vdata_H
EMIT
XEMIT
G1
Vdata
200
PVDD
b2
tft1
a2
B
b5
tft3
a5
OLED
PVEE
c2
c5
b6
tft2
a6
c6
Cst
C
b4
tft4
a4
A
b3
tft5
a3
REF
c4
a1
c3
tft6
c1
b1
Data
G1
EMIT
XEMIT

FIG. 9

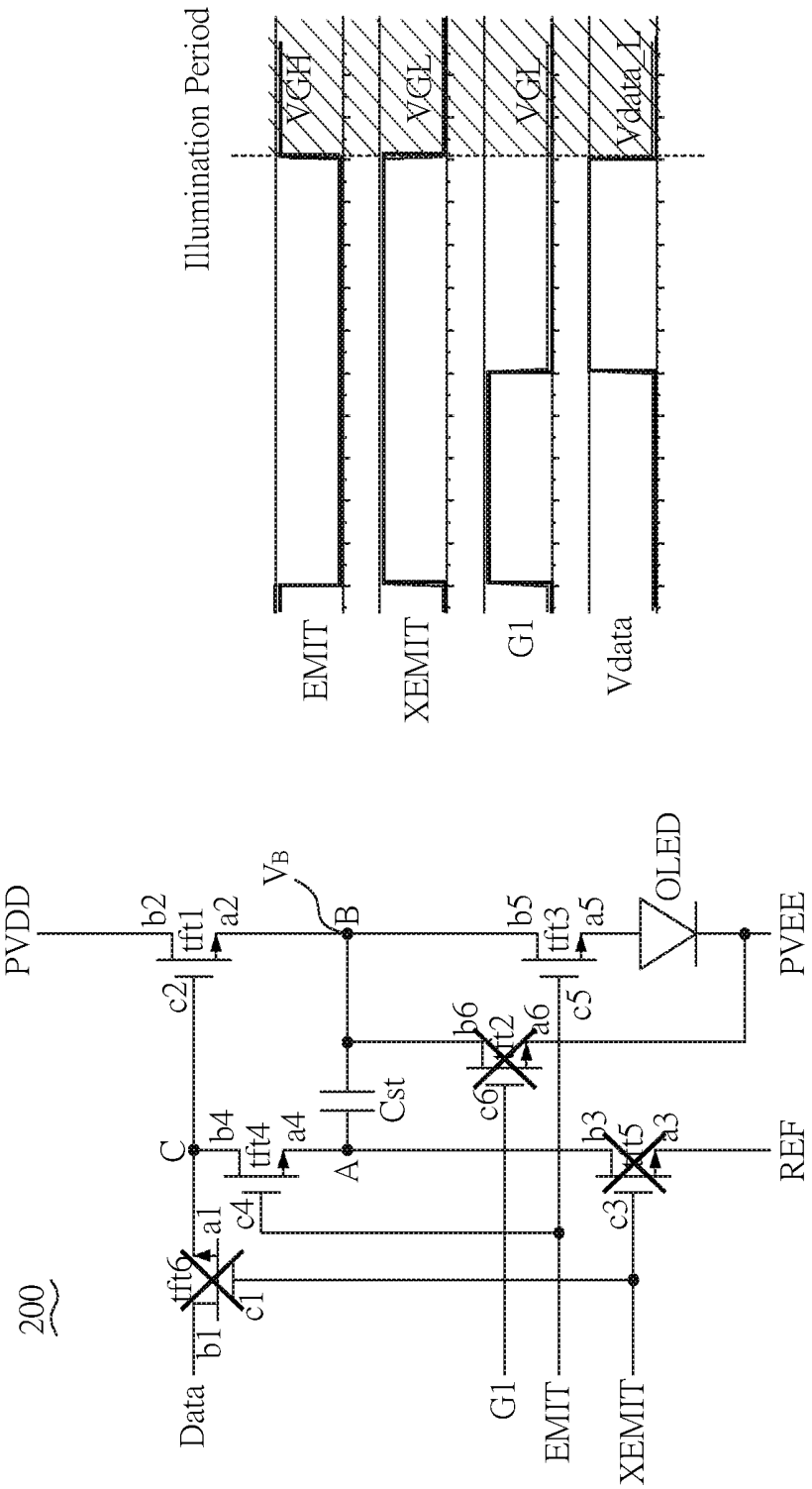

Illumination Period
VGH
VGL
VGL
Vdata_1
EMIT
XEMIT
G1
Vdata
200
PVDD
b2
tft1
a2
$V_B$
B
b5
tft3
a5
OLED
PVEE
c2
b6
tft2
a6
c5
C
b4
tft4
a4
Cst
A
c6
b3
tft5
a3
REF
c4
a1
tft6
c1
c3
b1
Data
G1
EMIT
XEMIT

FIG. 10

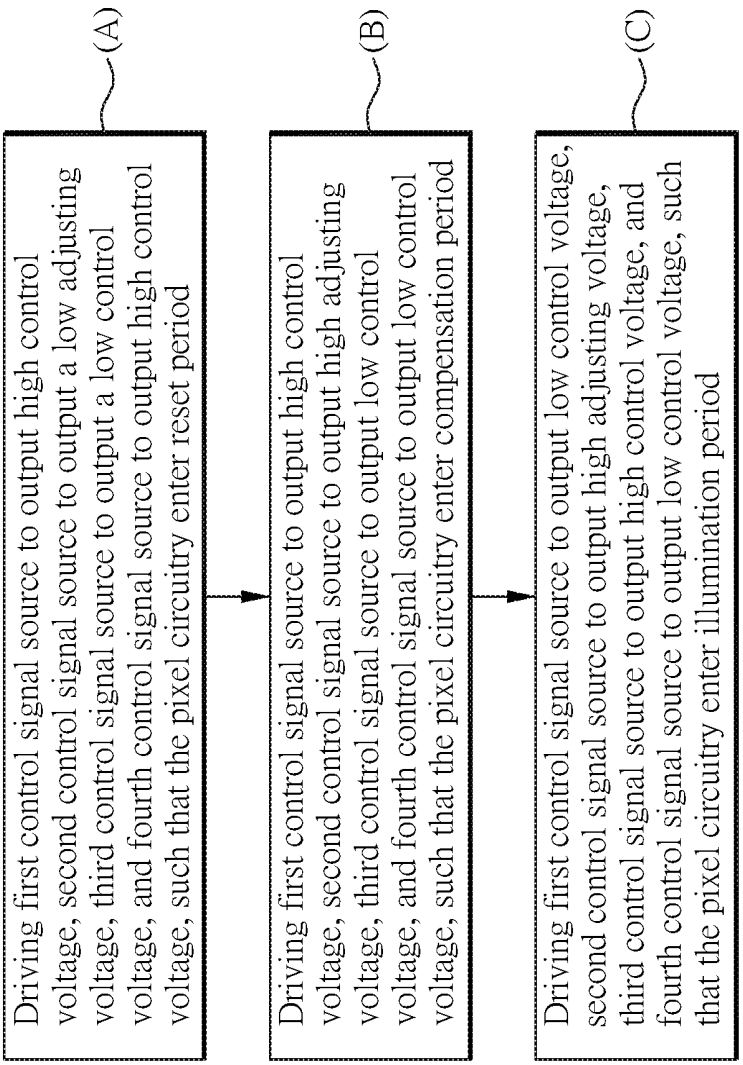

(A)
Driving first control signal source to output high control voltage, second control signal source to output a low adjusting voltage, third control signal source to output a low control voltage, and fourth control signal source to output high control voltage, such that the pixel circuitry enter reset period
(B)
Driving first control signal source to output high control voltage, second control signal source to output high adjusting voltage, third control signal source to output low control voltage, and fourth control signal source to output low control voltage, such that the pixel circuitry enter compensation period
(C)
Driving first control signal source to output low control voltage, second control signal source to output high adjusting voltage, third control signal source to output high control voltage, and fourth control signal source to output low control voltage, such that the pixel circuitry enter illumination period

FIG. 11

# LIGHT-EMITTING DIODE DISPLAY PANEL AND DRIVING METHOD THEREOF

## BACKGROUND

### 1. Field of the Disclosure

**[0001]** The present disclosure is related to the field of display device, and more specifically, the present disclosure is related to a LED display panel and the driving method thereof.

### 2. Description of Related Art

**[0002]** Driving transistors for the pixels in active matrix light-emitting diodes (AM-LED) can be divided into P-type and N-type according to the fabrication technique of the back plate. For conventional N-type driving transistor, threshold voltage deviation tends to occur in the driving transistor. In other words, the threshold voltage (Vt) for N-type driving transistor may vary locally because of fabrication process. That is to say, for two N-type driving transistors of the same size, when the same driving voltage is applied thereto, the output currents from the driving transistors may not be the same as each other, thereby causing problems such as uneven brightness (mura) or bad uniformity. Hence, conventional LED display panels still have plenty of room for improvement.

## SUMMARY

**[0003]** To this aim, the present disclosure provides a LED display panel and the driving method thereof. During the illumination period, the current of the driving transistor is not dependent on the threshold voltage thereof, and therefore, the current of the driving transistor is not affected by the variation of the threshold voltage. For two driving transistors of the same size, when the same driving voltage is applied thereto, the output currents from the driving transistors may be the same as each other, thereby solving problems such as uneven brightness (mura) or bad uniformity.

**[0004]** According to one aspect of the present disclosure, a LED display panel is provided, which may be disposed with a plurality of pixel circuitries. At least one pixel circuitry may include a data transistor, a driving transistor, a storage capacitor, a compensating transistor, a first control transistor, and a second control transistor. The data transistor may include a control terminal connected to a first control signal source, a first terminal connected to a data line, and a second terminal. The driving transistor may include a control terminal, a first terminal, and a second terminal connected to a high voltage source. The storage capacitor may be connected to the second terminal of the data transistor and the first terminal of the driving transistor. The compensating transistor may include a control terminal connected to the first control signal source, a first terminal connected to the control terminal of the driving transistor, and a second terminal connected to a second control signal source. The first control transistor may include a control terminal connected to a third control signal source, a first terminal connected to the second terminal of the data transistor, and a second terminal connected to the control terminal of the driving transistor. The second control transistor may include a control terminal connected to third control signal source, a first terminal connected to a light-emitting diode element, and a second terminal connected to the first terminal of the driving transistor.

**[0005]** According to another aspect of the present disclosure, a LED display panel is further provided, which may be disposed with a plurality of pixel circuitries. At least one pixel circuitry may include a data transistor, a driving transistor, a compensating transistor, a first control transistor, a storage capacitor, a second control transistor, and a reset transistor. The data transistor may include a control terminal connected to a first control signal source, a first terminal, and a second terminal connected to a data line. The driving transistor may include a control terminal connected to the first terminal of the data transistor, a first terminal, and a second terminal connected to a high voltage source. The compensating transistor may include a control terminal connected to the first control signal source, a first terminal connected to a reference signal, and a second terminal. The first control transistor may include a control terminal connected to a second control signal source, a first terminal connected to the second terminal of the compensating transistor, and a second terminal connected to the control terminal of the driving transistor. The storage capacitor may be connected to the second terminal of the compensating transistor and the first terminal of the driving transistor. The second control transistor may include a control terminal connected to the second control signal source, a first terminal connected to a light-emitting diode element, and a second terminal connected to the first terminal of the driving transistor. The reset transistor may include a control terminal connected to a third control signal source, a first terminal connected to a low voltage source, and a second terminal connected to the first terminal of the driving transistor.

**[0006]** According to yet another aspect of the present disclosure, a method for driving the LED display panel is provided. The LED display panel may be disposed with a plurality of pixel circuitries. The pixel circuitries may be arranged in rows and columns to form a plurality of regions. The method may use a first control signal source, a second control signal source, a third control signal source, and a fourth control signal source to control each pixel circuitry. The first control signal source, the second control signal source, the third control signal source, and the fourth control signal source may generate relevant control time sequence respectively, and each pixel circuitry has a reset period, a compensation period, and an illumination period. The reset period, the compensation period, and the illumination period may operate independently, and during the compensation period, the storage capacitor in each pixel circuitry may be charged with the voltage for displaying data, threshold voltage of the driving transistor, or high adjusting voltage of the control signal.

**[0007]** Other objects, advantages, and novel features of the disclosure will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0008]** FIG. **1** is a schematic diagram of the of the light-emitting diode (LED) display panel of the present disclosure;

**[0009]** FIG. **2** is a circuit diagram of the pixel circuitry of the present disclosure;

**[0010]** FIG. **3** is a schematic diagram of the reset period of the pixel circuitry of the present disclosure;

**[0011]** FIG. **4** is a schematic diagram of the compensation period of the pixel circuitry of the present disclosure;

**[0012]** FIG. **5** is a schematic diagram of the illumination period of the pixel circuitry of the present disclosure;

**[0013]** FIG. **6** is another circuit diagram of the pixel circuitry of the present disclosure;

**[0014]** FIG. **7** is another circuit diagram of the pixel circuitry of the present disclosure;

**[0015]** FIG. **8** is a schematic diagram of the reset period of the pixel circuitry of FIG. **7** of the present disclosure;

**[0016]** FIG. **9** is a schematic diagram of the compensation period of the pixel circuitry of FIG. **7** of the present disclosure;

**[0017]** FIG. **10** is a schematic diagram of the illumination period of the pixel circuitry of FIG. **7** of the present disclosure; and

**[0018]** FIG. **11** is a flowchart for the driving method of the LED display panel of the present disclosure.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

**[0019]** FIG. **1** is a schematic diagram of the of the light-emitting diode (LED) display panel of the present disclosure. The LED display panel **100** may be disposed with a plurality of pixel circuitries **200** and wirings that correspond to each other and are electrically connected; the pixel circuitries **200** may be arranged in rows and columns to form a plurality of regions. The pixel circuitries **200** may be adapted to drive the corresponding light-emitting diode elements to display image. In an embodiment of the present disclosure, the light-emitting diode element may be, but not limited to, organic light-emitting diode ((SLED). In some embodiments, the light-emitting diode element may be an inorganic light-emitting diode (LED), a quantum dot light-emitting diode (QLED), or other self-illuminating light-emitting diodes.

**[0020]** FIG. **2** is a circuit diagram of the pixel circuitry of the present disclosure. As shown in FIG. **2**, the pixel circuitry **200** may include a data transistor tft**6**, a driving transistor tft**1**, a storage capacitor Cst, a compensating transistor tft**5**, a first control transistor tft**4**, a second control transistor tft**3**, and a reset transistor tft**2**. Although the light-emitting diode element OLED in FIG. **2** is illustrated as an organic light-emitting diode, the present disclosure is not limited thereto.

**[0021]** As illustrated in FIG. **2**, the data transistor tft**6** may include a control terminal c**1**, a first terminal a**1**, and a second terminal b**1**. Particularly, the control terminal c**1** may be connected to the first control signal source G**2**, and the first terminal a**1** may be connected to the data line Data. The driving transistor tft**1** may include a control terminal c**2**, a first terminal a**2**, and a second terminal b**2**. The second terminal b**2** may be connected to the high voltage source PVDD. The storage capacitor Cst may be connected to the second terminal b**1** of the data transistor tft**6** and the first terminal a**2** of the driving transistor tft**1**. In other words, the storage capacitor Cst may be connected between node A and node B.

**[0022]** The compensating transistor tft**5** may include a control terminal c**3**, a first terminal a**3** and a second terminal b**3**. More specifically, the control terminal c**3** may be connected to the first control signal source G**2**, the first terminal a**3** may be connected to the control terminal c**2** of the driving transistor tft**1**, and the second terminal b**3** may be connected to the second control signal source VI. The first control transistor tft**4** may include a control terminal c**4**, a first terminal a**4** and a second terminal b**4**. Particularly, the control terminal c**4** may be connected to the third control signal source EMIT, the first terminal a**4** may be connected to the second terminal b**1** of the data transistor tft**6**, and the second terminal b**4** may be connected to the control terminal c**2** of the driving transistor tft**1**.

**[0023]** The second control transistor tft**3** may include a control terminal c**5**, a first terminal a**5**, and a second terminal b**5**. The control terminal c**5** may be connected to the third control signal source EMIT, the first terminal a**5** may be connected to an organic light-emitting diode element OLED (emitting layer comprises organic light-emitting material), and the second terminal b**5** may be connected to the first terminal a**2** of the driving transistor tft**1**. The reset transistor tft**2** may include a control terminal c**6**, a first terminal a**6** and a second terminal b**6**. More specifically, the control terminal c**6** may be connected to the fourth control signal source G**1**, the first terminal a**6** may be connected to the first terminal a**2** of the driving transistor tft**1**, and the second terminal b**6** may be connected to the low voltage source PVEE.

**[0024]** As shown in FIG. **2**, the data transistor tft**6**, the driving transistor tft**1**, the compensating transistor tft**5**, the first control transistor tft**4**, the second control transistor tft**3**, and the reset transistor tft**2** may all be N-type transistors. The semiconductor material for the data transistor tft**6**, the driving transistor tft**1**, the compensating transistor tft**5**, the first control transistor tft**4**, the second control transistor tft**3**, and the reset transistor tft**2** may be N-type Low Temperature Poly-silicon (LTPS), N-type Indium Gallium Zinc Oxide (IGZO), or N-type Amorphous Silicon, but the present disclosure is not limited thereto.

**[0025]** FIG. **3** is a schematic diagram of the reset period of the pixel circuitry of the present disclosure. Referring to FIG. **3**, during a reset period, the first control signal source G**2** may output a high control voltage VGH, the second control signal source VI may output a low adjusting voltage VI_L, the third control signal source EMIT may output a low control voltage VGL, and the fourth control signal source G**1** may output the high control voltage VGH. The high control voltage VGH may be higher than the voltage of the high voltage source PVDD. The low adjusting voltage VI_L may be higher than the voltage of the low voltage source PVEE. The low voltage source PVEE may be higher than the voltage of the low control voltage VGL.

**[0026]** During the reset period, since the first control signal source G**2** outputs the high control voltage VGH and the fourth control signal source G**1** outputs the high control voltage VGH, the data transistor tft**6**, the compensating transistor tft**5**, and the reset transistor tft**2** may be turned on, and voltages at both terminals of the storage capacitor Cst may respectively be Vdata and PVEE, where Vdata is a voltage for a display data written by the data line Data, and PVEE is a voltage of the low voltage source. In other words, the voltage at node A is Vdata while the voltage at node B is PVEE.

**[0027]** Because the third control signal source EMIT outputs low control voltage VGL, the first control transistor tft**4** and the second control transistor tft**3** may be turned off. The compensating transistor tft**5** may be turned on, and the voltage at node C may be the low adjusting voltage VI_L. In order to turn off the driving transistor tft**1**, the low adjusting voltage VI_L has to be low, so as to prevent current leakage

from occurring in the organic light-emitting diode element OLED. In one embodiment, the value of the low adjusting voltage VI_L has to be lower than the sum of the low voltage source voltage PVEE and the threshold voltage Vt**1** of the driving transistor tft**1**. During the reset period, there is no electrical path inside the organic light-emitting diode element OLED, and hence, dark-state light leakage and power consumption issues of the organic light-emitting diode element OLED can be avoided. The low adjusting voltage VI_L is higher than the low control voltage VGL, and the low adjusting voltage VI_L is lower than the sum of voltage of the low voltage source PVEE and the threshold voltage Vt**1** of the driving transistor tft**1** So, the low adjusting voltage VI_L satisfies the relationship VGL<VI_L<PVEE±Vt**1**.

**[0028]** FIG. **4** is a schematic diagram of the compensation period of the pixel circuitry of the present disclosure. Referring to FIG. **4**, during a compensation period, the first control signal source G**2** may output the high control voltage VGH, the second control signal source VI may output a high adjusting voltage VI_H, the third control signal source EMIT may output a low control voltage VGL, and the fourth control signal source G**1** may output the low control voltage VGL. The high voltage source PVDD may be higher than the high adjusting voltage VI_H.

**[0029]** During the compensation period, since the first control signal source G**2** outputs the high control voltage VGH, the compensating transistor tft**5** and the data transistor tft**6** may be turned on. Because the third control signal source EMIT outputs low control voltage VGL, the first control transistor tft**4** and the second control transistor tft**3** may be turned off. The fourth control signal source G**1** may output the low control voltage VGL, and the reset transistor tft**2** may be turned off. The compensating transistor tft**5** may be turned on and the first control transistor tft**4** may be turned off; therefore the voltage at node C is the high adjusting voltage Vl_H, and this causes the driving transistor tft**1** to be turned on. The voltage at node B is Vl_H−Vt**1**, where Vl_H is the high adjusting voltage of the second control signal source Vl, and Vt**1** is the threshold voltage of the driving transistor tft**1**. Since the data transistor tft**6** is turned on, the voltage at node A is Vdata. Therefore, the voltages at both sides of the storage capacitor Cst are Vdata and VI_H−Vt**1** respectively. In other words, the voltage in the storage capacitor Cst is Vdata−VI_H+Vt**1**.

**[0030]** FIG. **5** is a schematic diagram of the illumination period of the pixel circuitry of the present disclosure. Referring to FIG. **5**, during a illumination period, the first control signal source G**2** may output the low control voltage VGL, the second control signal source VI may output a high adjusting voltage VI_H, the third control signal source EMIT may output a high control voltage VGH, and the fourth control signal source G**1** may output the low control voltage VGL.

**[0031]** During the illumination period, since the first control signal source G**2** outputs the low control voltage VGL, the compensating transistor tft**5** and the data transistor tft**6** may be turned off. The fourth control signal source G**1** may output the low control voltage VGL, and the reset transistor tft**2** may be turned off. Because the third control signal source EMIT outputs low control voltage VGL, the first control transistor tft**4** and the second control transistor tft**3** may be turned on. Since the first control transistor tft**4** is turned on, the voltage at node C may equal to the voltage at node A, and the driving transistor tft**1** may be turned on.

**[0032]** During this time, an electrical path is formed between the high voltage source PVDD and the low voltage source PVEE. The voltage at node B is determined by the resistance of the driving transistor tft**1**, the second control transistor tft**3** and the organic light-emitting diode element OLED. The voltage at node B is labeled as $V_B$, and $V_B$=[(PVDD−PVEE)*(R**2**+R**3**)/(R**1**+R**2**+R**3**)]+PVEE, where PVDD is the output voltage of the high voltage source PVDD, PVEE is the output voltage of the low voltage source PVEE, R**1** is the resistance of the driving transistor tft**1** while the driving transistor tft**1** is turned on, R**2** is the resistance of the second control transistor tft**3** while the second control transistor tft**3** is turned on, and R**3** is the resistance of the organic light-emitting diode element OLED while the organic light-emitting diode element OLED is turned on. Since the voltage at the driving transistor tft**1** and the second control transistor tft**3** can be regarded as constant, and since R**1** is significantly larger than R**2**, the voltage $V_B$ at node B can be regarded as approximately the voltage of the organic light-emitting diode element OLED.

**[0033]** Since the voltage at node A equals to the voltage at node B plus the voltage in the storage capacitor Cst, the voltage at node A is $V_B$+Vdata−VI_H+Vt**1**. Similarly, the voltage at node C is $V_B$+Vdata−VI_H+Vt**1**. Therefore, the gate-source voltage Vgs_tft**1** of the driving transistor tft**1** is the voltage at node C minus the voltage at node B. Hence, the gate-source voltage Vgs_tft**1** of the driving transistor is ($V_B$+Vdata−VI_H+Vt**1**)−$V_B$=Vdata−VI_H+Vt**1**. In other words, the potential difference between both sides of the storage capacitor is Vdata−VI_H+Vt**1**. It can be appreciated that the voltage $V_B$ at node B does not appear in the equation for the current, and thus does not affect the current.

**[0034]** Therefore, during the illumination period, the current of the driving transistor tft**1** is:

$$I_{tft1}=I_{OLED}=Kpn[Vgs\_tft1-Vt1]^2=Kpn*[(Vdata-VI\_H+Vt1)-Vt1]^2=Kpn*[Vdata-VI\_H]^2,$$

**[0035]** where Kpn is the transistor transconductance parameter of the driving transistor tft**1**, Kpn=½*u*Cox*W/L; u is the charge carrier mobility of the semiconductor, Cox is the capacitance per unit area, and W/L is the transistor width-length ratio.

**[0036]** From the equations above, it can be appreciated that during the illumination period, the current $I_{\_tft1}$ of the driving transistor tft**1** is not affected by the threshold voltage Vt**1** of the driving transistor tft**1**. Therefore, the current $I_{\_tft1}$ of the driving transistor tft**1** is not affected by the localized threshold voltage variation that is caused by the fabrication process or any other factors. For two N type driving transistors of the same size, with the technique of the present disclosure, when the same driving voltage is applied thereto, the output currents from the driving transistors may be the same as each other, thereby solving problems such as uneven brightness (mura) or bad uniformity.

**[0037]** Furthermore, according to the equation for current, Vdata is a voltage for a display data written by the data line Data, i.e. Vdata corresponds to the current of the organic light-emitting diode element OLED, or Vdata corresponds to the brightness of the organic light-emitting diode element OLED; therefore, by writing in a voltage value of the display data, the brightness of the organic light-emitting diode element OLED can be changed. In addition, it can be appreciated from the equation for current that the brightness of the organic light-emitting diode element OLED can be changed via the high adjusting voltage VI_H. The high

adjusting voltage VI_H is a global parameter. In other words, when the high adjusting voltage VI_H is reduced, the brightness of the LED display panel **100** may be increased; when the high adjusting voltage VI_H is increased, the brightness of the LED display panel **100** may be reduced.

**[0038]** FIG. **6** is another circuit diagram of the pixel circuitry **200** of the present disclosure; the major difference between FIG. **6** and FIG. **2** lies in that the second terminal b**6** of the reset transistor tft**2** is connected to a reset signal source RESET. Therefore, during the reset period, the value of the low adjusting voltage VI_L has to be lower than the sum of the reset signal source RESET and the threshold voltage Vt**1** of the driving transistor tft**1**, such that the driving transistor tft**1** is turned off. Therefore, during the reset period, there is no electrical path inside the organic light-emitting diode element OLED, and hence, dark-state light leakage and power consumption issues of the organic light-emitting diode element OLED can be avoided.

**[0039]** The circuit in FIG. **6** is used to perform circuit simulation, the simulation conditions are: PVDD=4.6V, PVEE=−3.2V, VI_H=4.6V, VI_L=−3.2V, VRESRT=−3.2V, Vdata=0 to 4V, VGH=7V, VGL=−7V, $I_{tft1}$=47 nA, and Cst=100 fF. When the threshold voltage Vt**1** change is 0V, $I_{tft1}$ is 47.7011 nA, and the error is 0.00%. When the threshold voltage Vt**1** change is 0.1V, $I_{tft1}$ is 47.3786 nA, and the error is −0.68%. When the threshold voltage Vt**1** change is −0.1V, $I_{tft1}$ is 48.1941 nA, and the error is 1.03%.

**[0040]** Another simulation conditions are: PVDD=4.6V, PVEE=−3.2V, VI_H=4.6V, VI_L=−3.2V, VRESRT=−3.2V, Vdata=0 to 4V, VGH=7V, VGL=−7V, $I_{tft1}$=70 nA, and Cst=100 fF. When the threshold voltage Vt**1** change is 0V, $I_{tft1}$ is 70.346 nA, and the error is 0.00%. When the threshold voltage Vt**1** change is 0.1V, is 69.6632 nA, and the error is −0.97%. When the threshold voltage Vt**1** change is −0.1V, $I_{tft1}$ is 70.9798 nA, and the error is 0.90%.

**[0041]** Another simulation conditions are: PVDD=5.5V, PVEE=−3.2V, VI_H=0.4V, VI_L=−3.2V, VRESRT=−1V, Vdata=0 to 2V, VGH=7V, VGL=−7V, $I_{tft1}$=40 nA, and Cst=60 fF. When the threshold voltage Vt**1** change is 0V, $I_{tft1}$ is 40.592 A, and the error is 0.00%. When the threshold voltage Vt**1** change is 0.1V, $I_{tft1}$ is 39.4073 nA, and the error is −2.92%. When the threshold voltage Vt**1** change is −0.1V, $I_{tft1}$ is 41.7403 nA, and the error is 2.83%.

**[0042]** It is apparent from the aforementioned data that, although there is error in the current, such error is caused by the leakage of the transistor or the organic light-emitting diode element; alternatively, smaller capacitance of the storage capacitor Cst may magnify the effect of current leakage, thus causing the current error to be larger; the current error will be even higher if the technique of the present disclosure is not employed. Since the threshold voltage Vt**1** change is normally less than approximately 0.1V, from the simulation results, it can be shown that, for two N type driving transistors of the same size, with the technique of the present disclosure, when the same driving voltage is applied thereto, the error of output currents may be less than 1%, thereby solving problems such as uneven brightness (mura) or bad uniformity.

**[0043]** FIG. **7** is a circuit diagram of another pixel circuitry **200** of the present disclosure. As shown in FIG. **7**, the pixel circuitry **200** may include a data transistor tft**6**, a driving transistor tft**1**, a storage capacitor Cst, a compensating transistor tft**5**, a first control transistor tft**4**, a second control transistor tft**3**, and a reset transistor tft**2**. Although the light-emitting diode element OLED in FIG. **7** is illustrated as an organic light-emitting diode, the present disclosure is not limited thereto.

**[0044]** As illustrated in FIG. **7**, the data transistor tft**6** may include a control terminal c**1**, a first terminal a**1**, and a second terminal b**1**. Particularly, the control terminal c**1** may be connected to the first control signal source XEMIT, and the second terminal b**1** may be connected to the data line Data. The driving transistor tft**1** may include a control terminal c**2**, a first terminal a**2**, and a second terminal b**2**. More specifically, the control terminal c**2** is connected to the first terminal a**1** of the data transistor tft**6**, and the second terminal b**2** is connected to a high voltage source PVDD.

**[0045]** The compensating transistor tft**5** may include a control terminal c**3**, a first terminal a**3** and a second terminal b**3**. Particularly, the control terminal c**3** may be connected to the first control signal source XEMIT, and the first terminal a**3** may be connected to a reference signal REF. The first control transistor tft**4** may include a control terminal c**4**, a first terminal a**4** and a second terminal b**4**. Particularly, the control terminal c**4** may be connected to the second control signal source EMIT, the first terminal a**4** may be connected to the second terminal b**3** of the compensating transistor tft**5**, and the second terminal b**4** may be connected to the control terminal c**2** of the driving transistor tft**1**. In other words, the second terminal b**4** of the first control transistor tft**4** may be connected to the control terminal c**2** of the driving transistor tft**1** through a node C.

**[0046]** The storage capacitor Cst may be connected to the second terminal b**3** of the compensating transistor tft**5** and the first terminal a**2** of the driving transistor tft**1**. In other words, the storage capacitor Cst may be connected between node A and node B.

**[0047]** The second control transistor tft**3** may include a control terminal c**5**, a first terminal a**5**, and a second terminal b**5**. The control terminal c**5** may be connected to the second control signal source EMIT, the first terminal a**5** may be connected to an organic light-emitting diode element OLED, and a second terminal b**5** may be connected to the first terminal a**2** of the driving transistor tft**1**. The reset transistor tft**2** may include a control terminal c**6**, a first terminal a**6** and a second terminal b**6**. In particular, the control terminal c**6** may be connected to a third control signal source G**1**, the first terminal a**6** may be connected to a low voltage source PVEE, and the second terminal b**6** may be connected to the first terminal a**2** of the driving transistor tft**1**.

**[0048]** As shown in FIG. **7**, the data transistor tft**6**, the driving transistor tft**1**, the compensating transistor tft**5**, the first control transistor tft**4**, the second control transistor tft**3**, and the reset transistor tft**2** may all be N-type transistors. The semiconductor material for the data transistor tft**6**, the driving transistor tft**1**, the compensating transistor tft**5**, the first control transistor tft**4**, the second control transistor tft**3**, and the reset transistor tft**2** may be N-type Low Temperature Poly-silicon (LTPS), N-type Indium Gallium Zinc Oxide (IGZO), or N-type Amorphous Silicon, but the present disclosure is not limited thereto.

**[0049]** FIG. **8** is a schematic diagram of the reset period of the pixel circuitry **200** of FIG. **7** of the present disclosure. Referring to FIG. **8**, during a reset period, the first control signal source XEMIT is a high control voltage VGH, the second control signal source EMIT is a low control voltage VGL, and the third control signal source G**1** is the high control voltage VGH. The high control voltage VGH may be

higher than the voltage of the high voltage source PVDD. The low voltage source PVEE may be higher than the voltage of the low control voltage VGL.

**[0050]** During the reset period, since first control signal source XEMIT outputs the high control voltage VGH and the third control signal source G**1** outputs the high control voltage VGH, the compensating transistor tft**5**, the data transistor tft**6**, and the reset transistor tft**2** may be turned on, and voltages at both terminals of the storage capacitor Cst may respectively be VREF and PVEE, where VREF is a voltage for reference signal REF, and PVEE is a voltage of the low voltage source PVEE. In other words, the voltage at node A is VREF, the voltage at node B is PVEE, and the voltage at node C is Vdata, where Vdata is a voltage for a display data written by the data line Data. Under the circumstances, Vdata is low data voltage Vdata_L, and the voltage at node C is the low data voltage Vdata_L.

**[0051]** Because the second control signal source EMIT outputs low control voltage VGL, the first control transistor tft**4** and the second control transistor tft**3** may be turned off. The data transistor tft**6** may be turned on, and the voltage at node C may be the low data voltage Vdata_L. In order to turn off the driving transistor tft**1**, the low data voltage Vdata_L has to be low, so as to prevent current leakage from occurring in the organic light-emitting diode element OLED. In one embodiment, the value of the low voltage source Vdata_L has to be lower than the sum of the low voltage source voltage PVEE and the threshold voltage Vt**1** of the driving transistor tft**1**, so that the driving transistor tft**1** is turned off. During the reset period, since there is no electrical path inside the organic light-emitting diode element OLED, dark-state light leakage and power consumption issues of the organic light-emitting diode element OLED can be avoided. The low data voltage Vdata_L is higher than the low control voltage VGL, and the low data voltage Vdata_L is lower than the sum of voltage of the low voltage source PVEE and the threshold voltage Vt**1** of the driving transistor tft**1**. So, the low data voltage Vdata_L satisfies the relationship VGL<Vdata_L<PVEE+Vt**1**.

**[0052]** FIG. **9** is a schematic diagram of the compensation period of the pixel circuitry **200** of FIG. **7** of the present disclosure. Referring to FIG. **9**, during a compensation period, the first control signal source XEMIT outputs high control voltage VGH, the second control signal source EMIT outputs a low control voltage VGL, and the third control signal source G**1** outputs the low control voltage VGL.

**[0053]** During the compensation period, since the first control signal source XEMIT outputs the high control voltage VGH, the compensating transistor tft**5** and the data transistor tft**6** may be turned on. Because the second control signal source EMIT outputs low control voltage VGL, the first control transistor tft**4** and the second control transistor tft**3** may be turned off. The third control signal source G**1** may output the low control voltage VGL, and the reset transistor tft**2** may be turned off.

**[0054]** Since the data transistor tft**6** is turned on and the first control transistor tft**4** is turned off, the voltage at node C is Vdata, where Vdata is a voltage for a display data written by the data line Data. Under the circumstances, the Vdata is high data voltage Vdata_H, and the voltage at node C is the high data voltage Vdata_H; hence the driving transistor tft**1** is turned on. The voltage at node B is Vdata_H−Vt**1**, where Vdata_H is the voltage of the high data voltage Vdata_H, and Vt**1** is the threshold voltage of the driving transistor tft**1** Since the compensating transistor tft**5** is turned on, the voltage at node A is VREF. Therefore, the voltages at both sides of the storage capacitor Cst are VREF and Vdata_H−Vt**1** respectively. In other words, the voltage in the storage capacitor Cst is VREF−Vdata_H+Vt**1**.

**[0055]** FIG. **10** is a schematic diagram of the illumination period of the pixel circuitry **200** of FIG. **7** of the present disclosure. Referring to FIG. **10**, during a illumination period, the first control signal source XEMIT outputs low control voltage VGL, the second control signal source EMIT outputs the high control voltage VGH, and the third control signal source G**1** outputs the low control voltage VGL.

**[0056]** During the illumination period, since the first control signal source XEMIT outputs the low control voltage VGL, the compensating transistor tft**5** and the data transistor tft**5** may be turned off. The third control signal source G**1** may output the low control voltage VGL, and the reset transistor tft**2** may be turned off. Because the second control signal source EMIT outputs high control voltage VGH, the first control transistor tft**4** and the second control transistor tft**3** may be turned on. Since the first control transistor tft**4** is turned on, the voltage at node C may equal to the voltage at node A, and the driving transistor tft**1** may be turned on.

**[0057]** During this time, an electrical path is formed between the high voltage source PVDD and the low voltage source PVEE. The voltage at node B is determined by the resistance of the driving transistor tft**1**, the second control transistor tft**3** and the organic light-emitting diode element OLED. The voltage at node B is labeled as $V_B$, and $V_B$=[(PVDD−PVEE)*(R**2**+R**3**)/(R**1**+R**2**+R**3**)]+PVEE, where PVDD is the output voltage of the high voltage source PVDD, PVEE is the output voltage of the low voltage source PVEE, R**1** is the resistance of the driving transistor tft**1** while the driving transistor tft**1** is turned on, R**2** is the resistance of the second control transistor tft**3** while the second control transistor tft**3** is turned on, and R**3** is the resistance of the organic light-emitting diode element OLED while the organic light-emitting diode OLED element is turned on. Since the voltage at the driving transistor tft**1** and the second control transistor tft**3** can be regarded as constant, the voltage $V_B$ at node B can be regarded as the voltage of the organic light-emitting diode element OLED.

**[0058]** Since the voltage at node A equals to the voltage at node B plus the voltage in the storage capacitor Cst, the voltage at node A is $V_B$+VREF−Vdata_H+Vt**1**. Similarly, the voltage at node C is $V_B$+VREF−Vdata_H+Vt**1**. Therefore, the gate-source voltage Vgs_tft**1** of the driving transistor tft**1** is the voltage at node C minus the voltage at node B. Hence, the gate-source voltage Vgs_tft**1** of the driving transistor is ($V_B$+VREF−Vdata_H+Vt**1**)−$V_B$=VREF−Vdata_H+Vt**1**. In other words, the potential difference between both sides of the storage capacitor is VREF−Vdata_H+Vt**1**. It can be appreciated that the voltage $V_B$ at node B does not appear in the equation for the current, and thus does not affect the current.

**[0059]** Therefore, during the illumination period, the current of the driving transistor tft**1** is:

$$I_{\_tft1} = I_{\_OLED} = Kpn * [\mathrm{Vgs\_tft1} - Vt1]^2$$

-continued

$$= Kpn * [(VREF - \text{Vdata\_H} + Vt1) - Vt1]^2$$

$$= Kpn * [VREF - \text{Vdata\_H}]^2,$$

**[0060]** where Kpn is the transistor transconductance parameter of the driving transistor tft**1**, Kpn=½*u*Cox*W/L; u is the charge carrier mobility of the semiconductor, Cox is the capacitance per unit area, and W/L is the transistor width-length ratio.

**[0061]** From the equations above, it can be appreciated that during the illumination period, the current $I_{tft1}$ of the driving transistor tft**1** is not affected by the threshold voltage Vt**1** of the driving transistor tft**1**. Therefore, the current $I_{tft1}$ of the driving transistor tft**1** is not affected by the localized threshold voltage variation that is caused by the fabrication process or any other factors. For two N type driving transistors of the same size, with the technique of the present disclosure, when the same driving voltage is applied thereto, the output currents from the driving transistors may be the same as each other, thereby solving problems such as uneven brightness (mura) or bad uniformity.

**[0062]** Furthermore, according to the equation for current, Vdata_H is the high data voltage for a display data written by the data line Data, i.e. Vdata_H corresponds to the current of the organic light-emitting diode element OLED, or Vdata_H corresponds to the brightness of the organic light-emitting diode element OLED; therefore, by writing in a voltage value of the display data, the brightness of the organic light-emitting diode element OLED can be changed. In addition, it can be appreciated from the equation for current that the brightness of the organic light-emitting diode element OLED can be changed via the voltage VREF of the reference signal REF. The voltage VREF of the reference signal REF is a global parameter. In other words, when the voltage VREF of the reference signal REF is reduced, the brightness of the LED display panel **100** may be decreased; when the voltage VREF of the reference signal REF is increased, the brightness of the LED display panel **100** may be increased.

**[0063]** FIG. **11** is a flowchart for the driving method of the LED display panel of the present disclosure. Reference should also be made to the schematic diagram of LED display panel in FIG. **1**, and the circuit diagram of the pixel circuitry in FIG. **2** of the present disclosure. The LED display panel **100** may be disposed with a plurality of wirings and pixel circuitries **200** that correspond to each other and are electrically connected; the pixel circuitries **200** may be arranged in rows and columns. The method is to control each pixel circuitry **200** with a first control signal source G**2**, a second control signal source VI, a third control signal source EMIT and a fourth control signal source G**1**. The first control signal source G**2**, second control signal source VI, third control signal source EMIT, and fourth control signal source G**1** may generate their respective control signal sequentially, such that the pixel circuitry **200** has a reset period, a compensation period, and a illumination period. The reset period, the compensation period, and the illumination period may operate independently.

**[0064]** Step A: driving the first control signal source G**2** to output a high control voltage VGH, driving the second control signal source VI to output a low adjusting voltage VI_L, driving the third control signal source EMIT to output a low control voltage VGL, and driving the fourth control signal source G**1** to output the high control voltage VGH, such that the pixel circuitry **200** enter a reset period. The high control voltage VGH may be higher than the voltage of the high voltage source PVDD. The low adjusting voltage VI_L may be higher than the voltage of the low voltage source PVEE. The low voltage source PVEE may be higher than the voltage of the low control voltage VGL.

**[0065]** During the reset period, the data transistor tft**6**, the compensating transistor tft**5**, and the reset transistor tft**2** may be turned on, and voltages at both terminals of the storage capacitor Cst may respectively be Vdata and PVEE, where Vdata is a voltage for a display data written by the data line Data, and PVEE is a voltage of the low voltage source. In other words, as shown in FIG. **2**, the voltage at node A is Vdata while the voltage at node B is PVEE. The first control transistor tft**4** and the second control transistor tft**3** may be turned off. The compensating transistor tft**5** may be turned on, and the voltage at node C may be the low adjusting voltage VI_L. In order to turn off the driving transistor tft**1**, the value of the low adjusting voltage VI_L has to be smaller than the sum of the low voltage source PVEE and the threshold voltage Vt**1** of the driving transistor tft**1**, so as to prevent the current leakage from occurring in the organic light-emitting diode element OLED, and hence dark-state light leakage and power consumption issues of the organic light-emitting diode element OLED can be avoided. The low adjusting voltage VI_L is higher than the low control voltage VGL, and the low adjusting voltage VI_L is lower than the sum of voltage of the low voltage source PVEE and the threshold voltage Vt**1** of the driving transistor tft**1**. So, the low adjusting voltage VI_L satisfies the relationship VGL<VI_L<PVEE+Vt**1**.

**[0066]** Step B: driving the first control signal source G**2** to output a high control voltage VGH, driving the second control signal source VI to output a high adjusting voltage VI_H, driving the third control signal source EMIT to output a low control voltage VGL, and driving the fourth control signal source G**1** to output the low control voltage VGL, such that the pixel circuitry **200** enter a compensation period.

**[0067]** During the compensation period, the compensating transistor tft**5** and the data transistor tft**6** may be turned on, and the second control transistor tft**3** and the reset transistor tft**2** may be turned off. The compensating transistor tft**5** may be turned on and the first control transistor tft**4** may be turned off; therefore the voltage at node C in FIG. **2** is the high adjusting voltage Vl_H, and this turns the driving transistor tft**1** on. Therefore as shown in FIG. **2**, the voltage at node B is Vl_H−Vt**1**, where Vl_II is the high adjusting voltage of the second control signal source Vl, and Vt**1** is the threshold voltage of the driving transistor tft**1**. As shown in FIG. **2**, since the data transistor tft**6** is turned on, the voltage at node A is Vdata. Therefore, the voltages at both sides of the storage capacitor Cst are Vdata and VI_H−Vt**1** respectively. The voltage in the storage capacitor Cst is Vdata−VI_H+Vt**1**. In other words, during the compensation period, the storage capacitor Cst in each pixel circuitry may store the voltage Vdata of the display data, the threshold voltage Vt**1** of the driving transistor tft**1**, and high adjusting voltage VI_H of the control signal VI.

**[0068]** Step C: driving the first control signal source G**2** to output a low control voltage VGL, driving the second control signal source VI to output a high adjusting voltage VI_H, driving the third control signal source EMIT to output

a high control voltage VGH, and driving the fourth control signal source G**1** to output the low control voltage VGL, such that the pixel circuitry **200** enter a illumination period.

**[0069]** During the illumination period, the compensating transistor tft**5**, data transistor tft**6**, and reset transistor tft**2** may be turned off. The first control transistor tft**4**, second control transistor tft**3**, and driving transistor tft**1** may be turned on. The voltage in the storage capacitor Cst is Vdata−VI_H+Vt**1**, where Vdata is the voltage for display data written by the data line, Vl_H is the high adjusting voltage of the second control signal source Vl, and Vt**1** is the threshold voltage of the driving transistor tft**1**. The current of the driving transistor tft**1** is:

$$I_{tft1}=I_{OLED}=Kpn*[Vdata-VI\_H]^2,$$

**[0070]** where Kpn is the transistor transconductance parameter of the driving transistor tft**1**, Kpn=½*u*Cox*W/L; u is the charge carrier mobility of the semiconductor, Cox is the capacitance per unit area, and W/L is the transistor width-length ratio. In other words, during the illumination period, the current $I_{tft1}$ of the driving transistor tft**1** is not affected by the threshold voltage Vt**1** of the driving transistor tft**1**.

**[0071]** Apparently, with the technique of the present disclosure, the current of the driving transistor is not affected by the threshold voltage of the driving transistor. Therefore, the current of the driving transistor is less likely to be affected by the variation of threshold voltage. Therefore, for two N type driving transistors of the same size, when the same driving voltage is applied thereto, the output currents from the driving transistors may be the same as each other, thereby solving problems such as uneven brightness (mura) or bad uniformity.

**[0072]** Although the present disclosure has been explained in relation to its preferred embodiment, it is understood that many other possible modifications and variations can be made without departing from the spirit and scope of the disclosure as hereinafter claimed.

What is claimed is:

**1**. A display panel comprising a plurality of pixel circuitries, wherein at least one pixel circuitry comprises:

a data transistor comprising a control terminal connected to a first control signal source, a first terminal connected to a data line, and a second terminal;

a driving transistor comprising a control terminal, a first terminal, and a second terminal connected to a high voltage source;

a storage capacitor connected to the second terminal of the data transistor and the first terminal of the driving transistor;

a compensating transistor comprising a control terminal connected to the first control signal source, a first terminal connected to the control terminal of the driving transistor, and a second terminal connected to a second control signal source;

a first control transistor comprising a control terminal connected to a third control signal source, a first terminal connected to the second terminal of the data transistor, and a second terminal connected to the control terminal of the driving transistor; and

a second control transistor comprising a control terminal connected to the third control signal source, a first terminal connected to an organic light-emitting diode element, and a second terminal connected to the first terminal of the driving transistor.

**2**. The display panel of claim **1**, wherein the at least one circuitry further comprises a reset transistor comprising a control terminal connected to a fourth control signal source, a first terminal connected to the first terminal of the driving transistor, and a second terminal connected to a low voltage source.

**3**. The display panel of claim **2**, wherein the data transistor, the driving transistor, the compensating transistor, the first control transistor, the second control transistor, and the reset transistor are N-type transistors.

**4**. The display panel of claim **2**, wherein the data transistor, the driving transistor, the compensating transistor, the first control transistor, the second control transistor, and the reset transistor are made of N-type low temperature polysilicon (LTPS), N-type indium gallium zinc oxide (IGZO), or N-type amorphous silicon.

**5**. The display panel of claim **2**, wherein during a reset period, the data transistor, the compensating transistor, and the reset transistor are turned on, the driving transistor, and the first control transistor, and the second control transistor are turned off.

**6**. The display panel of claim **5**, wherein voltages at both terminals of the storage capacitor are respectively Vdata and PVEE, where Vdata is a voltage for a display data written by the data line, and PVEE is a voltage of the low voltage source.

**7**. The display panel of claim **2**, wherein during a compensation period, the driving transistor, the compensating transistor, and the data transistor are turned on, and the reset transistor, the first control transistor, and the second control transistor are turned off.

**8**. The display panel of claim **7**, wherein voltages at both terminals of the storage capacitor are respectively Vdata and VI_H−Vt**1**, where Vdata is a voltage for a display data written by the data line, VI_H is a high adjusting voltage from the second control signal source, and Vt**1** is a threshold voltage of the driving transistor.

**9**. The display panel of claim **2**, wherein each of the first control signal source and fourth control signal source is adapted to supply a high control voltage and a low control voltage, the second control signal source is adapted to supply a high adjusting voltage and a low adjusting voltage, the high control voltage is higher than a voltage of the high voltage source, the voltage of the high voltage source is higher than the high adjusting voltage, the low adjusting voltage is higher than a voltage of the low voltage source, and the voltage of the low voltage source is higher than the low control voltage.

**10**. A display panel comprising a plurality of pixel circuitries, wherein at least one pixel circuitry comprises:

a data transistor comprising a control terminal connected to a first control signal source, a first terminal, and a second terminal connected to a data line;

a driving transistor comprising a control terminal connected to the first terminal of the data transistor, a first terminal, and a second terminal connected to a high voltage source;

a compensating transistor comprising a control terminal connected to the first control signal source, a first terminal connected to a reference signal, and a second terminal;

a first control transistor comprising a control terminal connected to a second control signal source, a first terminal connected to the second terminal of the compensating transistor, and a second terminal connected to the control terminal of the driving transistor; and

a storage capacitor connected to the second terminal of the compensating transistor and the first terminal of the driving transistor;

a second control transistor comprising a control terminal connected to the second control signal source, a first terminal connected to an organic light-emitting diode element, and a second terminal connected to the first terminal of the driving transistor; and

a reset transistor comprising a control terminal connected to a third control signal source, a first terminal connected to a low voltage source, and a second terminal connected to the first terminal of the driving transistor.

**11**. The display panel of claim **10**, wherein the data transistor, the driving transistor, the compensating transistor, the first control transistor, the second control transistor, and the reset transistor are N-type transistors.

**12**. The display panel of claim **10**, wherein the data transistor, the driving transistor, the compensating transistor, the first control transistor, the second control transistor, and the reset transistor are made of N-type low temperature poly-silicon (LTPS), N-type indium gallium zinc oxide (IGZO), or N-type amorphous silicon.

**13**. The display panel of claim **10**, wherein during a reset period, the data transistor, the compensating transistor, and the reset transistor are turned on, and the driving transistor, the first control transistor, and the second control transistor are turned off.

**14**. The display panel of claim **13**, wherein voltages at both terminals of the storage capacitor are respectively VREF and PVEE, where VREF is a voltage for the reference signal, and PVEE is a voltage of the low voltage source.

**15**. The display panel of claim **10**, wherein during a compensation period, the driving transistor, the compensating transistor, and the data transistor are turned on, and the reset transistor, the first control transistor, and the second control transistor are turned off.

**16**. The display panel of claim **15**, wherein voltages at both terminals of the storage capacitor are respectively VREF and Vdata_H−Vt**1**, where VREF is a voltage for the reference signal, Vdata_H is a high data voltage for a display data written by the data line, and Vt**1** is a threshold voltage of the driving transistor.

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摘要(译)

本发明提供一种发光二极管显示面板及其驱动方法。数据晶体管包括连接到第一控制信号源的控制端子，连接到数据线的第一端子和第二端子。驱动晶体管包括控制端子，第一端子和连接到高压源的第二端子。存储电容器连接到数据和驱动晶体管。补偿晶体管包括连接到第一控制信号源的控制端，连接到驱动晶体管的控制端的第一端和连接到第二控制信号源的第二端。第一控制晶体管包括连接到第三控制信号源的控制端，连接到数据晶体管的第二端的第一端和连接到驱动晶体管的控制端的第二端。第二控制晶体管包括连接到第三控制信号源的控制端子，连接到有机发光二极管元件的第一端子，以及连接到驱动晶体管的第一端子的第二端子。